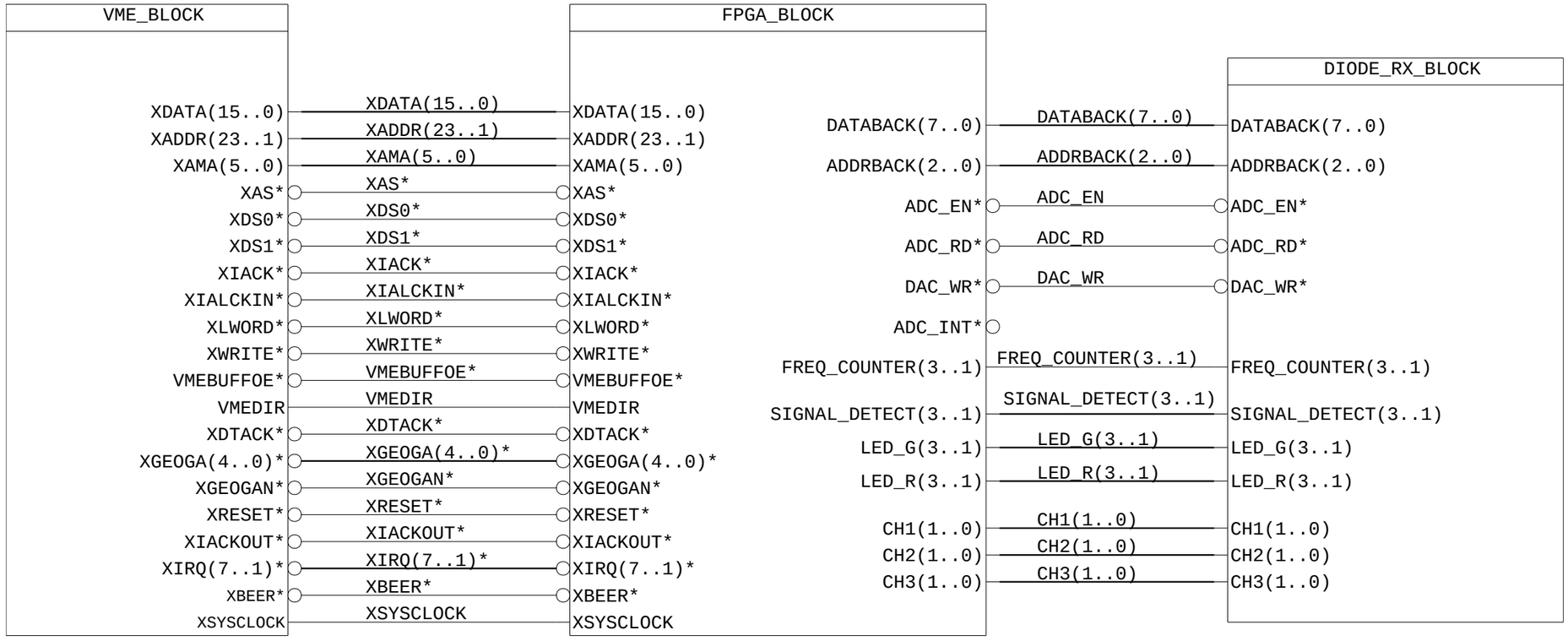


IMPORTANT NOTE: LT1763CS HAVE MAXIMUN OUTPUT OF 500 MA...
REQUIRED 375MA IN A APROXIMATE STIMATION MAYBE 400
THE TEXAS ONE OFFER 7.5 AMPS...
A DECISION OR A BETTER REGULATOR FOR 3.3 VOLTS MUST BE TAKEN

SEE NEXT PAGE
SEE NEXT PAGE
SEE NEXT PAGE
SEE NEXT PAGE

Project file:board.cpm SYSTEM: SPB16.3

EDA-01382-V4-1

TS/DEM
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

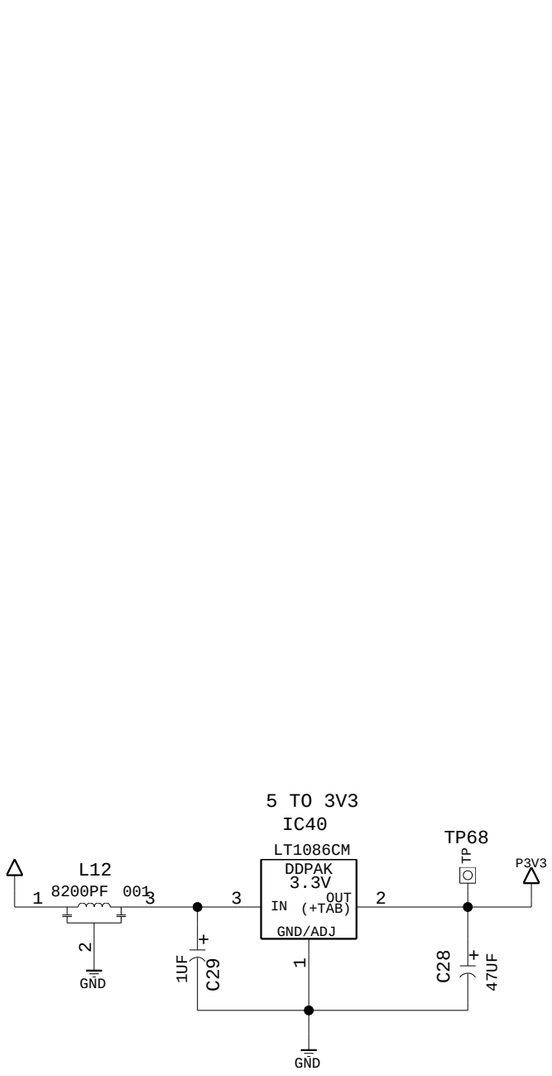
PROJECT:RF RX MODULE

MODULE:board Sheet: Module: 1/2 Project: 1/12

LAST_MODIFIED=Wed Jan 28 16:47:45 2015

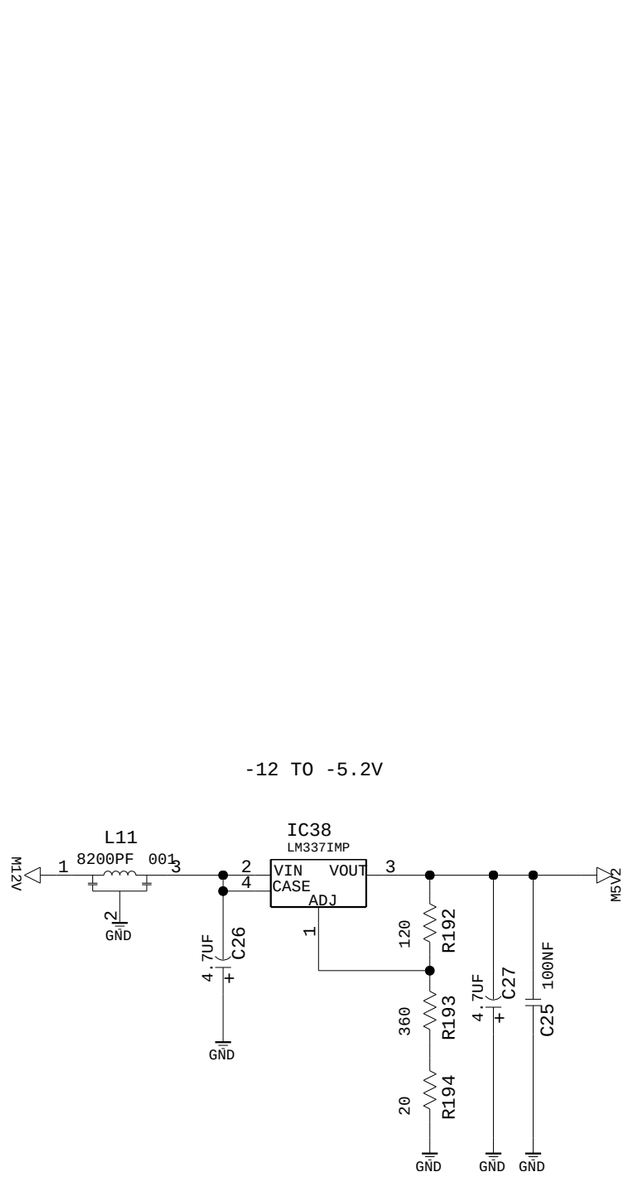
Design by: D. Stellfeld | PCB by: JMC | DATE: 28/01/2015

5 TO 3V3
IC40
LT1086CM
DDPAK
3.3V
IN (+TAB) OUT
GND/ADJ



5 TO 1V2 (SELEC DESIRED ONE)

-12 TO -5.2V



Project file:board.cpm			SYSTEM: SPB16.3
EDA-01382-V4-1	PROJECT:RF RX MODULE		
TS/DEM CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:board	Sheet: Module: 2/2 Project: 2/12	
	LAST_MODIFIED=Tue Apr 12 09:45:12 2016		
	Design by: D. Stellfeld	PCB by: JMC	DATE: 28/01/2015

J8

CONNVME P2

09031966921

D 31-16
A 31-24
E/S A 32-1
E/S C 32-1
+5
+5
+5
Reserve
0v
0v
0v
0v

DIN41612 FIXING SCREW?
4x SCREW BN5687-3061600
WASHER?
4x WASHER BN678-8303525 for M2.5 screw
NUT?
4x NUT BN628-1241427 for M2.5 screw

J7

CONVME64X P1

VMEDATA(15..0)
VMEADDR(23..1)
VMEAMA(5..0)
VMEDS0*
VMEDS1*
VMEIRQ(7..1)*
VMESYSCLOCK
VMERESET*
VMEBERR*
VMELWORD*
VMEWRITE*
VMEDTACKT*
VMEAS*
VMEIACK*
VMEIACKIN*
VMEIACKOUT*
VMEGEOGAN*
VMEGEOGA(4..0)*

5V FILTERING

TP43
L8 4000PF 008
F1 3.15A FH1
D5 15MQ040N
C15 47UF
C112 100NF
F2 1.25A FH2
F3 1.25A FH3
12VIN
M12VIN
GND
P3V3

R201 R200 R199 R198 R197 R196 10K

02 01 160 2101

VME_DRIVERS

VMEDATA(15..0) XDATA(15..0) IO
VMEDIR VMEDIR IN
VMEBUFFOE* VMEBUFFOE* IN
XSYSCLOCK XSYSCLOCK OUT
XBEER* XBEER* IN
XRESET* XRESET* OUT
XLWORD* XLWORD* OUT
XWRITE* XWRITE* OUT
XAS* XAS* OUT
XIACK* XIACK* OUT
XIALCKIN* XIALCKIN* OUT
XIACKOUT* XIACKOUT* IN
XDTACK* XDTACK* IN
VMEGEOGAN* XGEOGAN* OUT
VMEGEOGA(4..0)* XGEOGA(4..0)* OUT
VMEIRQ(7..1)* XIRQ(7..1)* IN
VMEDS1* XDS1* OUT
VMEDS0* XDS0* OUT
VMEAMA(5..0) XAMA(5..0) OUT
VMEADDR(23..1) XADDR(23..1) OUT

TP44 L9 12VIN D6 15MQ040N C113 1UF C16 47UF P12V GND

TP45 L10 M12VIN D7 15MQ040N C114 1UF C17 47UF M12V GND

R1 1M TOP_BORDER
R195 1M BOT_BORDER
GND

THE GND STRIP ALLOW THE DISCHARGE FROM THE FRONTPANEL TO THE GND CRATE THROUGH A 1M OHMS RESISTORS

METALLIC BORDERS CONNECTED TO GROUND

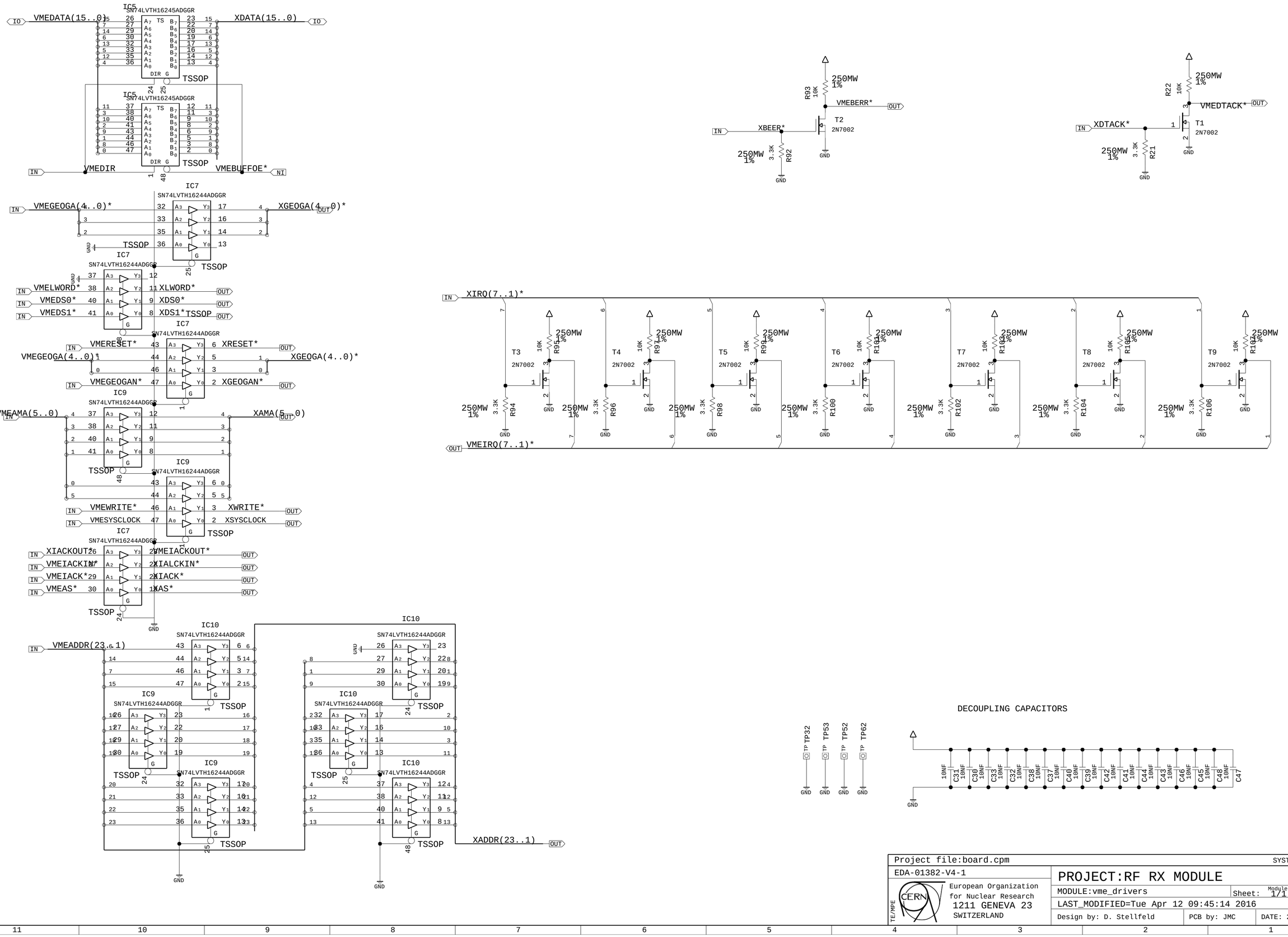
BLUE PARTS ARE NOT MOUNTED
(Components removed when the EDA-02287 "RF MODULE POWER SUPPLY FILTER'" is used)

Project file:board.cpm
SYSTEM: SPB16.3
EDA-01382-V4-1

TS/DEM
CERN
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND

PROJECT:RF RX MODULE

MODULE:vme_block
Sheet: Module: 1/1 Project: 3/12
LAST_MODIFIED=Tue Apr 12 09:45:13 2016
Design by: D. Stellfeld | PCB by: JMC | DATE: 28/01/2015



Project file:board.cpm		SYSTEM: SPB16.3
EDA-01382-V4-1	PROJECT:RF RX MODULE	
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:vme_drivers	Sheet: 1/1 Mqdule: / Project: 4/12
TE/MPE	LAST_MODIFIED=Tue Apr 12 09:45:14 2016	
	Design by: D. Stellfeld	PCB by: JMC — DATE: 28/01/2015

PORTS INTERCONNECTION
(DUE TO THE FPGA IS CHANGING
ALL TIME, I DECIDE DO THIS WAY
FOR NOT REDRAW THE CIRCUIT ALL
TIMES)

IN XRESET*
IO XDATA(15..0)
IN XSYSCLOCK
IN XADDR(23..1)
IN XAMA(5..0)
IN XAS*
IN XDS0*
IN XDS1*
IN XIACK*
IN XIALCKIN*
IN XLWORD*
IN XWRITE*
IN XGEOGA(4..0)*
IN XGEOGAN*

XIACKOUT* OUT
VMEBUFFOE* OUT
VMEDIR OUT
XDTACK* OUT
XIRQ(7..1)* OUT

IN FREQ_COUNTER(3..1)
IN ADC_INT*

ADDRBACK(2..0) OUT
ADC_EN* OUT
ADC_RD* OUT
DAC_WR* OUT

DATABACK(7..0) IO
XBEER* OUT

IN SIGNAL_DETECT(3..1)

LED_R(3..1) OUT
LED_G(3..1) OUT

CH1(1..0) OUT
CH2(1..0) OUT
CH3(1..0) OUT

DECOUPLING VCIO

C51 22NF, C50 22NF, C49 22NF, C73 22NF, C72 22NF, C70 22NF, C68 22NF, C67 22NF, C64 22NF, C63 22NF, C62 22NF, C61 22NF, C60 22NF, C59 22NF, C58 22NF, C56 22NF, C54 22NF, C1 22NF, C2 47UF, C7

GND

DECOUPLING VCCINT

P1V2

C52 22NF, C53 22NF, C57 22NF, C66 22NF, C69 22NF, C71 22NF, C55 22NF, C65 47UF, C10

GND

TP1 TP3 TP18 TP25

GND GND GND GND

BYTEBLASTER

J5

PROG_ASDO
PROG_NCS0
PROG_DATA0
PROG_NCE
PROG_NCONFIG
PROG_CONFIGDONE
PROG_DCLK

R205 10K, R202 10K, R208 10K

BARD2X5

GND

J4

PROG_TDI R203 10K
R206 22
PROG_TMS R204 10K
PROG_TDO
PROG_TCK R207 10K

BARD2X5

JTAG CONNECTOR

CONFIGURATION MEMORY

IC2 EPCS4

TP70 TP71 TP72
PROG_DCLK 6 DCLK
PROG_ASDO 5 ASDI
PROG_NCS0 1 CS
DATA 2 PROG_DATA0 TP75

R213 10K, R214 10K

PROG_MSEL0 TP73
PROG_MSEL1 TP74

PROG_NSTATUS 10K R46

R45 1M, C9 1UF, D4 1N4148_CMS, R215 620

PROG_INIT_DONE

PROG_DONE 1 SEC
CIRQUIT DELAY (R+C)
DO NOT SOLDER!!!!!

LD6 HSMS-C170

GND

THE OSCILLATOR IS 80MHZ
OSCILATOR REFERENCE: FARNEL(9713590)
MAKER: C-MAC
PACKAGE: THE SAME

VCC=P3V3FILTRE

L1 8200PF, QZ1 X392T 80MHz, EN/D OUT, 33 R20, TP69, CLK50MHZ

100NF C74

P3V3FILTRE\G

OSCILATOR XXMHZ

ATENTION!!!
RSMD JUMPERS
ONLY ONE OR NONE
(NOTHING FROM THE MOMENT)

IC8

XLWORD*	6	VMELWORDNA	VMEBUFOEN 15 VMEBUFFOE*
FPGA_RESET_N	8	RESETNA	TDO 16 PROG_TDO
XDS0*	10	VMEDS0NA	DCLK 21 PROG_DCLK
XDS1*	11	VMEDS1NA	NCE 22 PROG_NCE
XGEOGAN*	14	VMEGEON	NCONFIG 26 PROG_NCONFIG
PROG_TMS	17	TMS	VMEDIR 48 VMEDIR
PROG_TCK	18	TCK	VEMCOMM_G 72 VME_LED_G
PROG_TDI	19	TDI	VEMCOMM_R 74 VME_LED_R
PROG_DATA0	20	DATA0	ERROR_LED 75 ERROR_LED
XSYSCLOCK	23	XSYSCLOCK	OPFINISHEDOUT 77 DEB_OPFINISHED
CLK50MHZ	27	CLK	VMEDIRFLOAT 84 VMEDIRFLOAT
ADC_INT*	134	ADC_INTNA	NSTATUS 121 PROG_NSTATUS
XWRITE*	203	VMEWRITENA	CONF_DONE 123 PROG_CONFIGDONE
XIALCKIN*	206	IACKINNA	MSEL1 125 PROG_MSEL1
XIACK*	207	VMEIACKNA	MSEL0 126 PROG_MSEL0
XAS*	208	VMEASNA	ADC_ENNA 133 ADC_EN*
PROG_ASDO	1	ASDO	ADC_RDNA 135 ADC_RD*
PROG_NCS0	2	NCSO	DAC_WRNA 137 DAC_WR*
SIGNAL_DETECT(3..1)		SIGNAL_DETECT_IN<3..1>	XBERNA 152 XBEER*
XAMA(5..0)		VMEAMAIN<5..0>	VMEDTACKN 195 XDTACK*
CH1(1..0)		LASERMODID_IN_CH1<1..0>	IACKOUTNA 205 XIACKOUT*
CH2(1..0)		LASERMODID_IN_CH2<1..0>	INIT_DONE 107 PROG_INIT_DONE
CH3(1..0)		LASERMODID_IN_CH3<1..0>	NCEO 108
FREQ_COUNTER(3..1)		FREQ_COUNTERS<3..1>	ADDRBACK<2..0> ADDRBACK(2..0)
XADDR(23..1)		VMEADDRA<23..1>	DATABACK<7..0> DATABACK(7..0)
XGEOGA(4..0)*		VMEGEOADDR<4..0>	LEDR<3..1> LED_R(3..1)
ADDR_MOD_SELECT(7..0)		MODADDRSEL<7..0>	VMEINTREQN<7..1> XIRQ(7..1)
			VMESTATE<3..0> DEB_VMESTATE(3..0)
			VMEDATA<15..0> XDATA(15..0)
			LEDG<3..1> LED_G(3..1)

digital_rxv2

ONLY CAN BE CONNECT ONE AT TIME!!!
J1 ON: RESECT CIRCUIT ACTIVE
J2 ON: RESET CIRCUIT DEACTIVE

SOFTWARE RESET

PB1 3P, MAN_RESET_N

1N4448_SMD, 1N4148_CMS

R2 680, R3 10K, C35 1UF, C34 100NF

IC1 MAX6303CSA+

RST_IN SRT SWT VCC GND RST WDI WDS

XRESET TP2 PROG_INIT_DONE

FPGA_RESET_N TP5

POWER MONITOR CHECKER
THE MAX6303 WILL KEEP THE
FPGA IN RESET MODE AFTER
POWER ON DURING ONE SECOND

ONLY CAN BE CONNECT ONE AT TIME!!!
J1 ON: RESECT CIRCUIT ACTIVE
J2 ON: RESET CIRCUIT DEACTIVE

HARDWARE RESET

IC6 MAX6303CSA+

XRESET* R18 680, R19 10K, C3 100NF, C36 100NF

PROG_NCONFIG TP4

FROM FARNELL,

VME_LED_R 100 R4 LD1 CBI551-3009 100 VME_LED_G
ERROR_LED 100 R6 LD2 CBI551-3009 100 R7 R5

GND

(RESISTANCES FOR
OBTAIN A COURRENT OF 10MA
THROUGH THE DIODE)

DEBUGGER CONNECTOR

J6

VMEDIRFLOAT
DEB_VMESTATE(3..0)
DEB_OPFINISHED

HARWIN2X4FD

R15 R14 R17 R16 R11 R10 R13 R12 10K

SW1 BCH, SW2 BCH

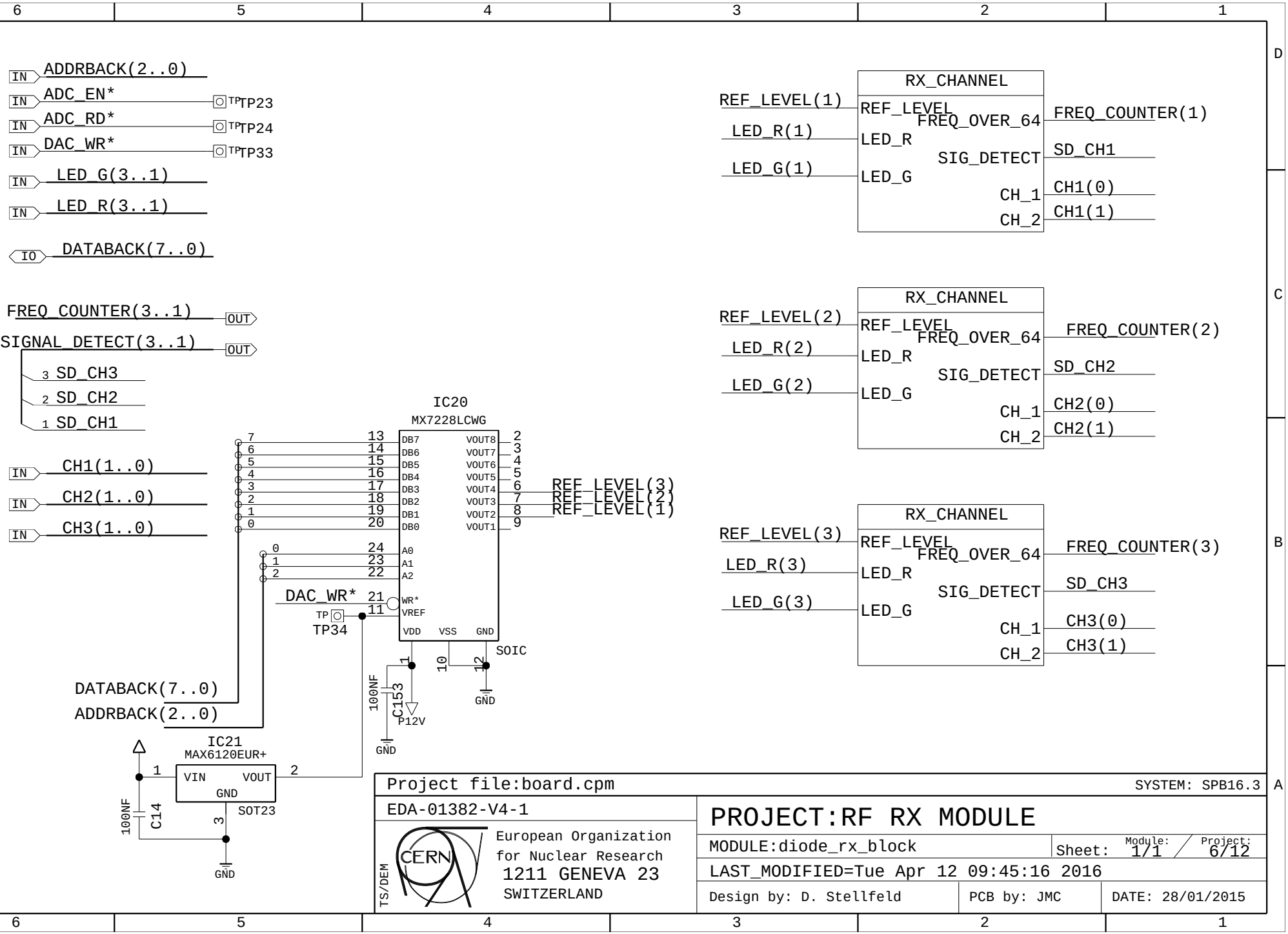
ADDR_MOD_SELECT(7..0)

SW2 MODULE ADDRES SWITCHS SELLECTION

Project file:board.cpm SYSTEM: SPB16.3
EDA-01382-V4-1
TE/MPE CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND

PROJECT:RF RX MODULE

MODULE:fpga_block Sheet: 1/1 Module: 1/1 Project: 5/12
LAST_MODIFIED=Tue Apr 12 09:45:15 2016
Design by: D. Stellfeld PCB by: JMC DATE: 28/01/2015



Project file:board.cpm

SYSTEM: SPB16.3

EDA-01382-V4-1

PROJECT:RF RX MODULE

European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TS/DEM

MODULE:diode_rx_block

Sheet: Module: 1/1 Project: 6/12

LAST_MODIFIED=Tue Apr 12 09:45:16 2016

Design by: D. Stellfeld | PCB by: JMC | DATE: 28/01/2015

THE PHOTODIODES ARE NOT SOLDERED DIRECTLY TO THE BOARD.
SOME MUST BE USED FOR MAKE THIS COMPONENTS EASY TO REMOVE.
REMEMBER, THE DIAMETER OF THE PHOTODIODES'S HOLES MUST BE 1.05MM

SHOCKET FOR THE LASER/PHOTODIODE
08.61.20.960.9
BANDE CONT.CARRIER

size=20
SOCKET
HARWIN_H3153F01

OCP or OSI LASERDIODE INC
SRX-03-ST-A-x-xx or TL2063PT-005STL

J1
SRX 03_PST
MOUNTED=NO
SIGNAL_DETECT+
SIGNAL_DETECT-
VPD
VCC
CASE
VEE
DATA+
DATA-

50 OHMS LINE
C237
C238
220PF
R209
R210
510
C239
100PF
100NF
C92
R28
R29
NOT MOUNTED
R38
R39
TP19
IC11
SIG_DETECT
SN65 LVDS34
OUT
TP20
TP21
R37
R40
L2
8200PF
R30
R31
FILTER MUST BE SITUATED
AS CLOSE AS POSSIBLE TO BOTH PHOTODIODES

50 OHMS LINE

MC100EP11DG
TP16
R54
R56
R55
R57
TP17
VCC VEE
SOIC

LVPECL COAX DRIVER
IC13
R51
R53
R50
R52
TP15
TP14
IC12
MC10EP89DG
VEE VCC
Q1 Q1* Q0 Q0*
TP12
TP13
SOIC

50 OHMS LINE
100NF
C8
33
R48
85SMA-50-0-144
PX1
150
R47
R49

FREQ_DIV_64
F_IN
F_IN*
F_OUT
FREQ_OVER_64
OUT
TP22

LD3
CBI551-3009
IN
LED_R
R211
100
LED_G
R212
NI

50 OHMS LINE
RX1
TRR-1B43
DOUT
VCC GND
C4
100NF
C5
C91
10NF
C6
1uF
R24
R26
R23
R25
R27
TP8
TP9
TP10
TP11
ADCMP561BRQZ
QSOP
IC4
ADCMP561
+IN
-IN
LE
LE*
Q
Q*
VDD
VCC
VEE
GND
L3
1UH
POW_POS
C88
C89
C13
10NF
100PF
1uF
25V

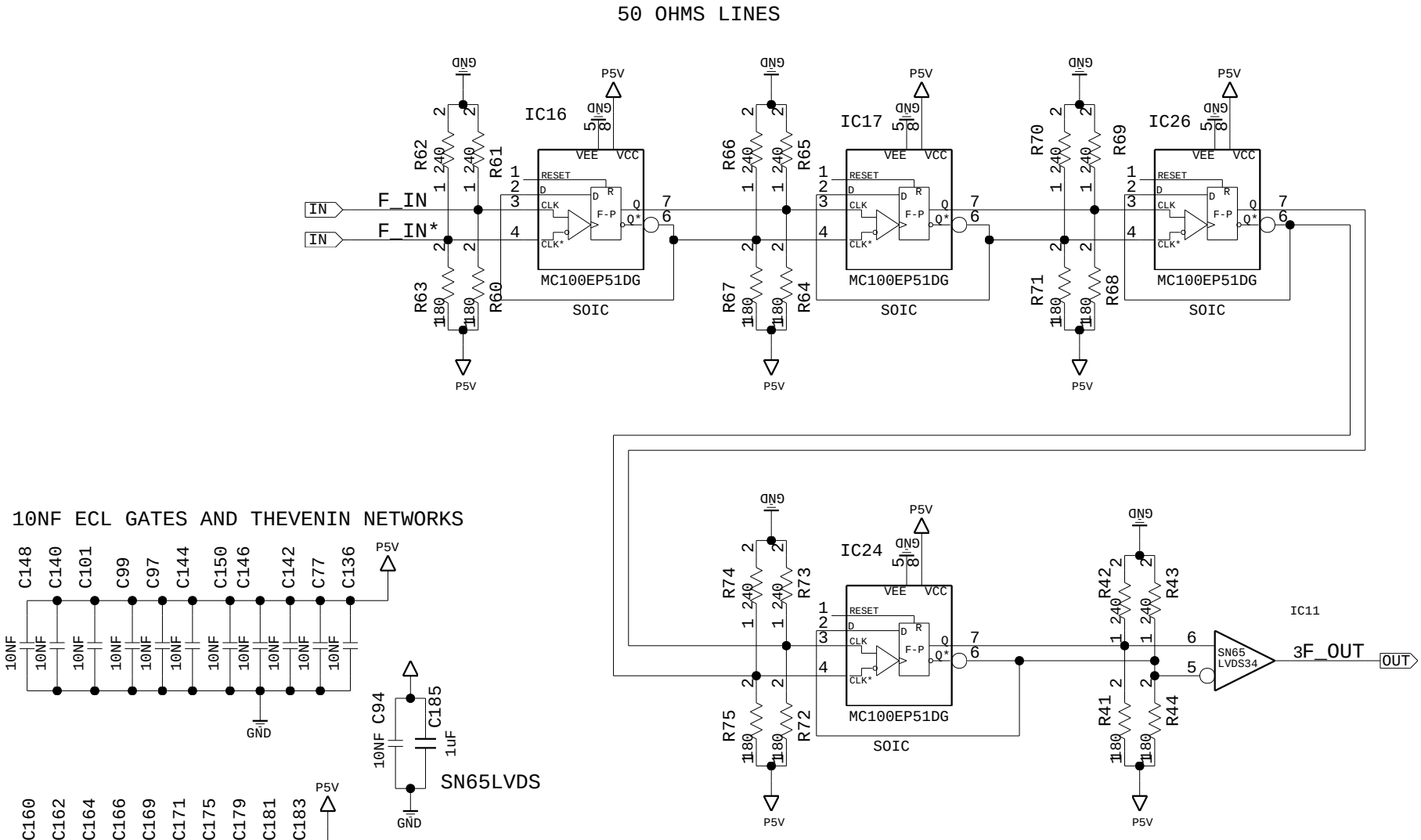
DAC POSTPROCESING (COMPRESING RANGE TO 1/2)
P12V
M12V
M5V2
TP6
TP7
REF_LEVEL
IN
C21
1uF 25V
R9
470K
POW_POS
C83
C84
100NF
10K
R8
IC3
TLE2061
V+
V-
IN+
IN-
OUT
N1
N2
20K
R34
R32
R33
IC4
ADCMP561BRQZ
QSOP

BCH
A6A_16RF
CH_2
CH_1
OUT
R36
R35
100K

C216 C95 C138 C75 C107 C110 C108 C109 C87 C103 C105 C76 C78 C80 C82 C85 C86 C90 C93 C96 C98
10NF
1uF

REMEMBER, THE DIAMETER OF THE PHOTODIODES'S HOLES MUST BE 1.05MM

Project file:board.cpm			SYSTEM: SPB16.3
EDA-01382-V4-1	PROJECT:RF RX MODULE		
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:rx_channel	Sheet: 1/1	Module: 1/1 Project: 7/12
TS/DEM	LAST_MODIFIED=Tue Apr 12 09:45:17 2016		
	Design by: D. Stellfeld	PCB by: JMC	DATE: 28/01/2015



Project file:board.cpm		SYSTEM: SPB16.3
EDA-01382-V4-1	PROJECT:RF RX MODULE	
TS/DEM CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:freq_div_64	Sheet: 1/1 Module: / Project: 8/12
	LAST_MODIFIED=Tue Apr 12 09:45:18 2016	
	Design by: D. Stellfeld	PCB by: JMC DATE: 28/01/2015

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REMEMBER, THE DIAMETER OF THE PHOTODIODES'S HOLES MUST BE 1.05MM

SHOCKET FOR THE LASER/PHOTODIODE
08.61.20.960.9
BANDE CONT.CARRIER

size=20
SOCKET
HARWIN_H3153F01

OCP or OSI LASERDIODE INC
SRX-03-ST-A-x-xx or TL2063PT-005STL

J2
SRX 03_PST
MOUNTED=NO
SIGNAL_DETECT+
SIGNAL_DETECT-
VPD
VCC
CASE
VEE
DATA+
DATA-

50 OHMS LINE
C240
C241
220PF
C242
100PF
100NF
C176
R218
R219
510
R113
R114
00

NOT MOUNTED
R81
R82
82
TP39
TP40
TP36
IC22
SIG_DETECT
SN65 LVDS34
OUT

R115
R116
L4
8200PF
001

FILTER MUST BE SITUATED
AS CLOSE AS POSSIBLE TO BOTH PHOTODIODES

50 OHMS LINE

MC100EP11DG
R129
R131
R130
R132
TP50
TP51
SOIC

IC25
R126
R128
R125
R127
120
TP49
TP48

LVPECL COAX DRIVER
IC14
MC10EP89DG
VEE
VCC
Q1
Q1*
Q0
Q0*
TP46
TP47
SOIC

50 OHMS LINE
C18
100NF
R123
33
PX2
85SMA-50-0-144
R122
R124
150
GND

FREQ_DIV_64
F_IN
F_IN*
F_OUT
FREQ_OVER_64
OUT
TP35

LD4
CBI551-3009
IN
LED_R
LED_G
NI
R216
R217
100

50 OHMS LINE

RX2
TRR-1B43
DOUT
VCC
GND
TP28
TP29
C11
C12
100NF
C159
10NF
C100
1uF
R108
R109
R111
R110
R112
TP30
TP31
ADCMP561BRQZ
QSOP
IC19
ADCMP561
+IN
-IN
LE
LE*
Q
Q*
VDD
VEE
M5V2
L5
1UH
POW_POS
C156
C157
C102
100PF
1uF 25V

DAC POSTPROCESING (COMPRESING RANGE TO 1/2)
P12V
TP26
REF_LEVEL
IN
C104
1uF 25V
470K
R59
100NF
C151
10K
R58
IC18
TLE2061
V+
V-
IN+
IN-
OUT
N1
N2
TP27
POW_POS
M12V
C152

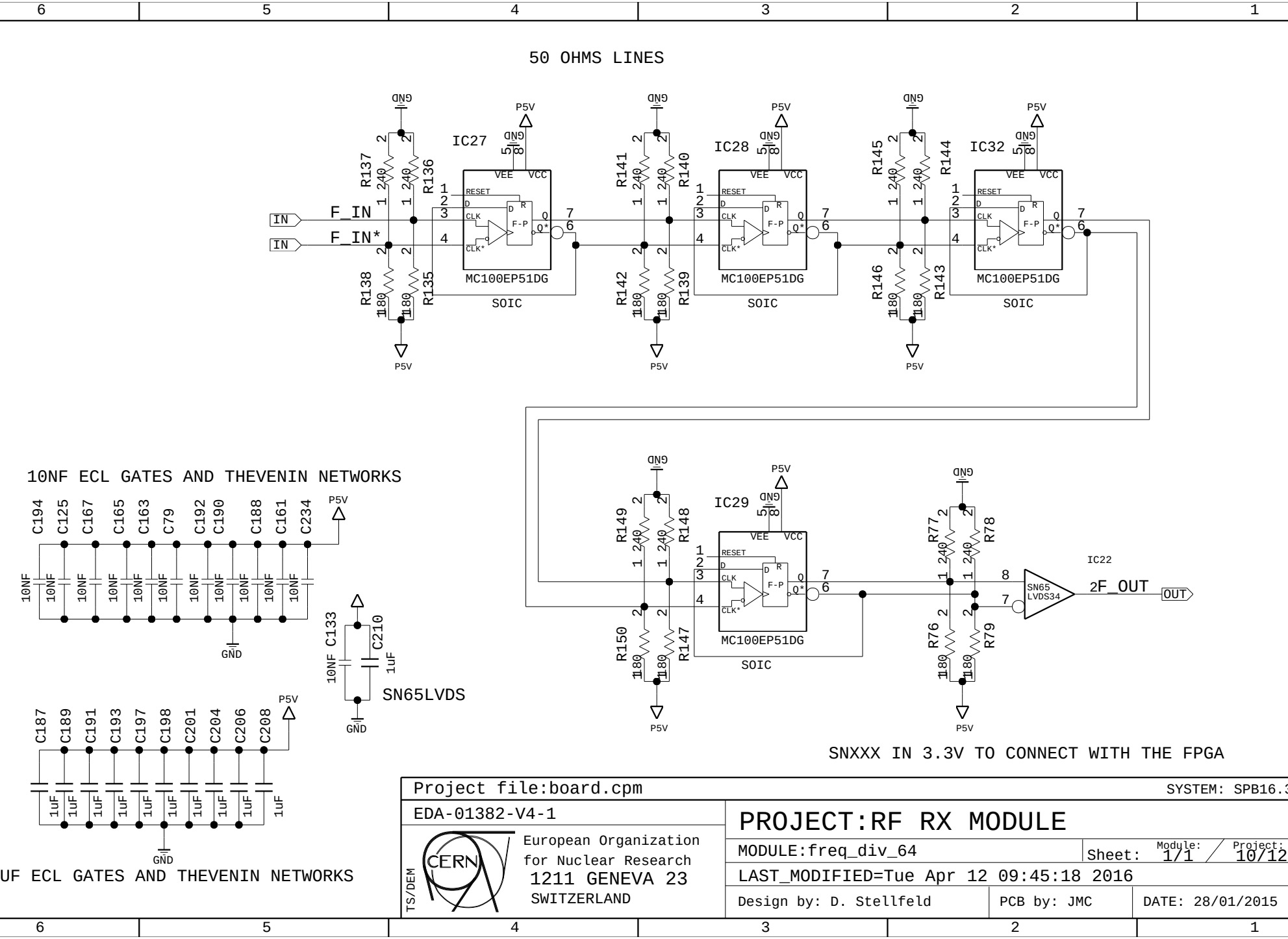
20K
R119
10K
R117
R118
IC19
ADCMP561BRQZ
QSOP

BCH
A6A_16RF
CH_2
CH_1
OUT
R121
R120
100K

C217
C180
C129
C174
C172
C186
C173
C184
C170
C182
C127
C106
C111
C115
C117
C119
C121
C124
C126
C128
C130
10NF
1uF

REMEMBER, THE DIAMETER OF THE PHOTODIODES'S HOLES MUST BE 1.05MM

Project file:board.cpm			SYSTEM: SPB16.3
EDA-01382-V4-1	PROJECT:RF RX MODULE		
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (TS/DEM)	MODULE:rx_channel	Sheet: Module: 1/1 Project: 9/12	
	LAST_MODIFIED=Tue Apr 12 09:45:17 2016		
	Design by: D. Stellfeld	PCB by: JMC	DATE: 28/01/2015


50 OHMS LINES
IC27
IC28
IC32
IC29
IC22
MC100EP51DG
SOIC
F_IN
F_IN*
IN
R137
R136
R138
R135
R141
R140
R142
R139
R145
R144
R146
R143
R149
R148
R150
R147
R77
R78
R76
R79
RESET
VEE
VCC
CLK
CLK*
F-P
GND
P5V
SN65
LVDS34
2F_OUT
OUT
10NF ECL GATES AND THEVENIN NETWORKS
C194
C125
C167
C165
C163
C79
C192
C190
C188
C161
C234
10NF
C133
C210
1uF
SN65LVDS
C187
C189
C191
C193
C197
C198
C201
C204
C206
C208
1UF ECL GATES AND THEVENIN NETWORKS
SNXXX IN 3.3V TO CONNECT WITH THE FPGA
Project file:board.cpm
SYSTEM: SPB16.3
EDA-01382-V4-1
PROJECT:RF RX MODULE
TS/DEM
CERN
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
MODULE:freq_div_64
Sheet: 1/1
Module:
Project: 10/12
LAST_MODIFIED=Tue Apr 12 09:45:18 2016
Design by: D. Stellfeld
PCB by: JMC
DATE: 28/01/2015

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SOME MUST BE USED FOR MAKE THIS COMPONENTS EASY TO REMOVE.
REMEMBER, THE DIAMETER OF THE PHOTODIODES'S HOLES MUST BE 1.05MM

SHOCKET FOR THE LASER/PHOTODIODE
08.61.20.960.9
BANDE CONT.CARRIER

size=20
SOCKET
HARWIN_H3153F01

OCP or OSI LASERDIODE INC
SRX-03-ST-A-x-xx or TL2063PT-005STL

J3
SRX 03_PST
MOUNTED=NO
SIGNAL_DETECT+
SIGNAL_DETECT-
DATA+
DATA-
VPD
VCC
CASE
VEE

50 OHMS LINE
C243
C244
220PF
R222
R223
510

C245
100PF
100NF
C203

NOT MOUNTED
R158
R159
L6
8200PF
001

NOT MOUNTED
R89
R90
TP41
TP42
TP38
IC23
SN65
LVDS34
SIG_DETECT
OUT

FILTER MUST BE SITUATED
AS CLOSE AS POSSIBLE TO BOTH PHOTODIODES

50 OHMS LINE
R154
R155

50 OHMS LINE

MC100EP11DG
R172
R174
TP65
R173
R175
TP66
VCC
VEE
SOIC

IC33
R169
R171
R168
R170
TP64
TP63

LVPECL COAX DRIVER
IC15
MC10EP89DG
TP60
TP61
VEE
VCC
SOIC

50 OHMS LINE
C24
100NF
R166
33
PX3
85SMA-50-0-144
R165
R167
150

FREQ_DIV_64
F_IN
F_IN*
F_OUT
FREQ_OVER_64
OUT
TP37

LD5
CBI551-3009
IN
LED_R
R220
100
LED_G
R221
NI

DAC POSTPROCESING (COMPRESING RANGE TO 1/2)
P12V
TP54
R134
10K
IC30
TLE2061
REF_LEVEL
C135
1uF
25V
R133
470K
TP55
POW_POS
M12V
C196
100NF

RX3
TRR-1B43
DOUT
VCC
GND
C202
10NF
C132
1uF

50 OHMS LINE
R151
R152
R156
TP56
TP57
TP58
TP59
C19
100NF
C20
R153
R157
ADCMP561BRQZ
QSOP
IC31
ADCMP561
L7
M5V2
1UH
POW_POS
C199
C200
100PF
C134
1uF
25V

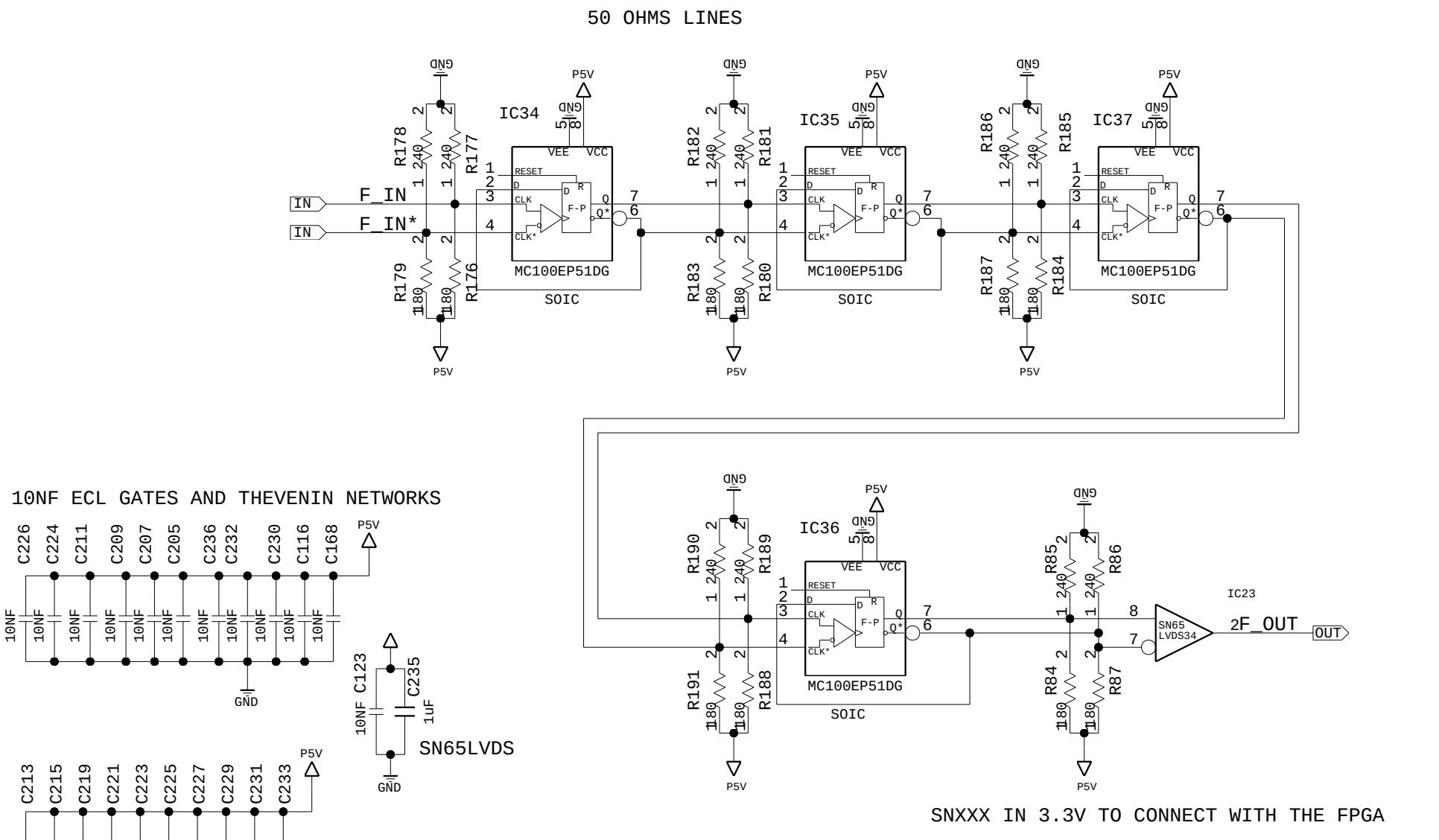
IC31
R162
20K
R160
10K
R161
10K
ADCMP561BRQZ
QSOP
M5V2

BCH
A6A_16RF
R164
100K
R163
100K
CH_2
CH_1
OUT

C131 C122 C118 C228 C214 C218 C81 C120 C222 C212 C220 C137 C139 C141 C143 C145 C147 C149 C154 C155 C158
10NF / 1uF

REMEMBER, THE DIAMETER OF THE PHOTODIODES'S HOLES MUST BE 1.05MM

Project file:board.cpm			SYSTEM: SPB16.3
EDA-01382-V4-1	PROJECT:RF RX MODULE		
TS/DEM CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:rx_channel	Sheet: 1/1	Module: 1/1 Project: 11/12
	LAST_MODIFIED=Tue Apr 12 09:45:17 2016		
	Design by: D. Stellfeld	PCB by: JMC	DATE: 28/01/2015



Project file:board.cpm		SYSTEM: SPB16.3
EDA-01382-V4-1	PROJECT:RF RX MODULE	
TS/DEM CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:freq_div_64	Sheet: 1/1 Module: / Project: 12/12
	LAST_MODIFIED=Tue Apr 12 09:45:18 2016	
	Design by: D. Stellfeld	PCB by: JMC DATE: 28/01/2015